UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/727,744	12/01/2000	Lawrence Richard Fontaine	RA 5312 (1028.1132101)	4178

27516 7590 08/24/2004

UNISYS CORPORATION
MS 4773
PO BOX 64942
ST. PAUL, MN 55164-0942

EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/727,744	FONTAINE ET AL.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-27 have been considered. Claims 1, 2, 10, and 11 have been amended as per Applicant's request.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 5-13, and 14-18 are rejected under 35 U.S.C. 102(e) as being taught by Col et al., U.S. Patent Number 6,338,136 (herein referred to as Col).

4. Referring to claim 1, Col has taught a method for storing a digital value to memory in a pipelined instruction processor, wherein the digital value is read from memory in response to a conditional jump instruction to determine if the condition of the conditional jump instruction is satisfied (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B), the method comprising:

a. Generating at least one status bit based on the digital value to be stored, the at least one status bit relating to a particular condition of a conditional jump instruction and specifying if the particular condition of the conditional jump

instruction is satisfied or not (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B); and

b. Storing the digital value and the at least one status bit to memory (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B).

5. Referring to claim 2, Col has taught wherein the conditional jump instruction reads the digital value and the at least one status bit from memory to determine if the condition of the conditional jump instruction is satisfied without having to submit the condition of the conditional jump instruction to an arithmetic logic stage of the pipeline's instruction processor (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B).

6. Referring to claim 3, Col has taught wherein the at least one status bit is read from memory at the same time as the digital value (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B).

7. Referring to claim 5, Col has taught wherein the at least one status bit is set high if the digital value is zero (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

8. Referring to claim 6, Col has taught wherein the at least one status bit is set high if the digital value is a positive value (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

9. Referring to claim 7, Col has taught wherein the at least one status bit is set high if the digital value is negative (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55;

column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

10. Referring to claim 8, Col has taught wherein the at least one status bit is set high if the digital value is a non zero value (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

11. Referring to claim 9, Col has taught wherein the at least one status bit is set high based on the value of the least significant bit of the digital value (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

12. Referring to claim 10, Col has taught in a pipelined instruction processor that executes instructions including conditional jump instructions, one or more of the conditional jump

instructions reading a digital value from memory to determine if the condition of the conditional jump instruction is satisfied (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B), the improvement comprising:

a. Status bit generator for generating at least one status bit based on a digital value, the at least one status bit indicating if a predetermined condition of a conditional jump instruction is satisfied (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B); and

b. Storing means for storing the digital value and the at least one status bit to the memory (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B).

13. Referring to claim 11, Col has taught wherein a selected conditional jump instruction reads the digital value and the at least one status bit from memory to determine if the condition of the conditional jump instruction is satisfied (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B).

14. Referring to claim 12, Col has taught wherein the at least one status bit is read from the memory at the same time as the digital value is read (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

15. Referring to claim 14, Col has taught wherein the at least one status bit is set high if the digital value is zero (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

16. Referring to claim 15, Col has taught wherein the at least one status bit is set high if the digital value is a positive value (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

17. Referring to claim 16, Col has taught wherein the at least one status bit is set high if the digital value is negative (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

18. Referring to claim 17, Col has taught wherein the at least one status bit is set high if the digital value is anon zero value (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

19. Referring to claim 18, Col has taught wherein the at least one status bit is set high based on the value of the least significant bit of the digital value (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B). In regards to Col, it is stated that a flag is set, this could mean the flag is set to high or low, it does not matter.

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Col et al., U.S. Patent Number 6,338,136 (herein referred to as Col), as applied to claims 1 and 10 above, in view of Olson et al., U.S. Patent Number 5,824,070 (herein referred to as Olson). Col has taught wherein the memory has one or more addressable locations (Col column 16, lines 48-53). Col has not taught the at least one status bit is stored at the same addressable location as the corresponding digital value. Olson has taught the at least one status bit is stored at the same addressable location as the corresponding digital value (Olson column 1, lines 36-40). A person of ordinary skill in the art at the time the invention was made, and as recognized in Olson, would have recognized that the status bits must be associated with the correct instruction to be

visible to the user (Olson column 1, lines 31-35). Therefore, a person of ordinary skill in the art at the time the invention was made would have incorporated the status bits of Olson in the device of Col in order to ensure the status bits are associated with the correct instruction.

22. Claims 19-22 and 24-27 rejected under 35 U.S.C. 103(a) as being unpatentable over Watson et al., U.S. Patent Number 3,573,854 (herein referred to as Watson) in view of Col et al., U.S. Patent Number 6,338,136 (herein referred to as Col).

23. Referring to claim 19, Watson has taught in a pipelined instruction processor that executes instructions including conditional jump instructions, the improvement comprising:

a. A plurality of addressable registers, each of the addressable registers (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5);

b. Logic to access a current instruction (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5);

c. A jump look-ahead controller for generating a jump look-ahead signal, the jump look-ahead signal is a function of the identified jump condition (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5);

d. Tracking logic for tracking the addresses of a predetermined number of previous instructions in the pipelined instruction processor and comparing the addresses of each previous instruction to the address of the current instruction to generate a series of jump disable signals (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5); and

e. Conflict detection logic for generating a jump early signal using the jump look-ahead signal and the series of jump disable signals, the jump early signal initiates the conditional jump depending on the values of the jump disable signals (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5).

24. Watson has not taught:

a. One or more of the conditional jump instructions reading a digital value from memory to determine if the condition of the conditional jump instruction is satisfied;

b. Storing a value that includes a digital value and at least one jump status bit;

c. Wherein the current instruction includes an address and a corresponding jump field, the address identifies one of the addressable registers and the corresponding jump field identifies a jump status bit of the at least one jump status bits within the identified addressable register; and

d. Using the address that identifies one of the addressable registers and the jump field that identifies a jump status bit within the identified addressable register.

25. Col has taught:

a. One or more of the conditional jump instructions reading a digital value from memory to determine if the condition of the conditional jump instruction is satisfied (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B);

b. Storing a value that includes a digital value and at least one jump status bit (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B);

c. Wherein the current instruction includes an address and a corresponding jump field, the address identifies one of the addressable registers and the corresponding jump field identifies a jump status bit of the at least one jump status bits within the identified addressable register (Col Abstract; column 1, lines 13-26; column 2,

lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B); and

d. Using the address that identifies one of the addressable registers and the jump field that identifies a jump status bit within the identified addressable register (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B).

26. A person of ordinary skill in the art at the time the invention was made, and as recognized in Col, would have recognized that compare-and-jump operations of Col execute without undue program delays (Col column 3, lines 41-43) and decreases the number of instructions (Col column 4, lines 3-6), thereby increasing overall processor efficiency. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the compare-and-jump operations of Col to increase processor efficiency.

27. Referring to claims 20 and 21, Watson has not taught

a. Wherein each jump status bit is dependent on the digital value stored in the corresponding addressable register; and

b. A bit status generator for generating the corresponding jump status bits.

28. Col has taught:

a. Wherein each jump status bit is dependent on the digital value stored in the corresponding addressable register (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B); and

b. A bit status generator for generating the corresponding jump status bits (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B).

29. A person of ordinary skill in the art at the time the invention was made, and as recognized in Col, would have recognized that compare-and-jump operations of Col execute without undue program delays (Col column 3, lines 41-43) and decreases the number of instructions (Col column 4, lines 3-6), thereby increasing overall processor efficiency. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the compare-and-jump operations of Col to increase processor efficiency.

30. Referring to claim 22, Watson has taught a prediction logic block responsive to the jump early signal for implementing a prediction algorithm to predict the conditional jump depending on the values of the jump disable signals (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5).

31. Referring to claim 24, Watson has taught wherein the predetermined number of instructions are sequentially piped through an execution pipeline after being piped through a pre-fetch pipeline, the execution pipeline includes a write-back stage (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5).

32. Referring to claim 25, Watson has taught wherein the addressable register is written during the write-back stage (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5).

33. Referring to claim 26, Watson has taught wherein the execution pipeline further includes an address generation stage, a present address stage, an output operand stage, a capture data stage, and an arithmetic operation stage, all before the write-back stage (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5).

34. Referring to claim 27, Watson has taught a method for determine if a condition of a conditional jump instruction is satisfied in a pipelined instruction processor, the method comprising:

a. Generating a jump look-ahead signal that is a function of the selected jump status bit read from the selected address location of the addressable memory, the identified jump status bit is accessed using the address and the jump field of the current instruction (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5);

b. Tracking the addresses of a predetermined number of previous instructions in the pipelined instruction processor and comparing the addresses to the address of the current instruction to generate a series of jump disable signals (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5); and

c. Generating a jump early signal using the jump look-ahead signal and the series jump disable signals, the jump early signal initiates a conditional jump depending on the value of the jump disable signals (Watson column 1, lines 40-63; column 1, lines 56-75; column 4, lines 37-47; column 4, line 68 to column 5, line 61; column 5, line 74 to column 6, line 37; column 6, lines 69-74; column 7, line 7 to column 8, line 13; Figure 4; and Figure 5).

35. Watson has not taught:

a. Storing a digital value and one or more jump status bits that are based on the digital value in each of a plurality of address locations in an addressable memory; and

b. Accessing a current instruction, the current instruction having an address and a jump field, the address identifies a selected address location of the addressable memory, and the jump field identifies a selected jump status bit of the selected address location.

36. Col has taught:

a. Storing a digital value and one or more jump status bits that are based on the digital value in each of a plurality of address locations in an addressable memory (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4, lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B); and

b. Accessing a current instruction, the current instruction having an address and a jump field, the address identifies a selected address location of the addressable memory, and the jump field identifies a selected jump status bit of the selected address location (Col Abstract; column 1, lines 13-26; column 2, lines 18-31 and 53-55; column 3, lines 20-43; column 3, line 50 to column 4, line 2; column 4,

lines 12-27; column 14, lines 34-36 and 51-61; column 15, lines 17-37 and 44-52; column 16, lines 20-27; column 16, line 48 to column 17, line 5; column 21, line 53 to column 22, line 6; column 22, lines 32-52; column 23, line 4 to column 24, line 14; Figures 5A to 5B).

37. A person of ordinary skill in the art at the time the invention was made, and as recognized in Col, would have recognized that compare-and-jump operations of Col execute without undue program delays (Col column 3, lines 41-43) and decreases the number of instructions (Col column 4, lines 3-6), thereby increasing overall processor efficiency. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the compare-and-jump operations of Col to increase processor efficiency.

38. Claim 23 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Watson in view of Col as applied to claim 19 above, and further in view of Heuring and Jordan's Computer Systems Design and Architecture ©1997 (herein referred to as Heuring). Watson in view of Col has not taught wherein the tracking logic includes a queue for sequentially storing a pre-determined number of instructions prior to sequentially piping the pre-determined number of instructions through a read stage and decode stage in a pre-fetch pipeline. Heuring has taught wherein the tracking logic includes a queue for sequentially storing a pre-determined number of instructions prior to sequentially piping the pre-determined number of instructions through a read stage and decode stage in a pre-fetch pipeline (Heuring Pages 92-95). A person of ordinary skill in the art at the time the invention was made would have recognized that pre-fetching increases the speed and efficiency of the processor. Therefore, it would have been obvious to a person of

ordinary skill in the art at the time this invention was made to incorporate the pre-fetching of Heuring to increase processor speed and efficiency.

Response to Arguments

39. Applicant's arguments with respect to claims 1-3, 5-12, and 14-27 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

40. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Col et al., U.S. Patent Number 6,330,657, has taught compressing instructions into one instruction for concurrent execution, specifically compare and jump instructions.

b. Col et al., U.S. Patent Number 6,647,489, has taught compressing instructions into one instruction for concurrent execution, specifically compare and jump instructions.

41. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

42. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

43. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
August 20, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100